

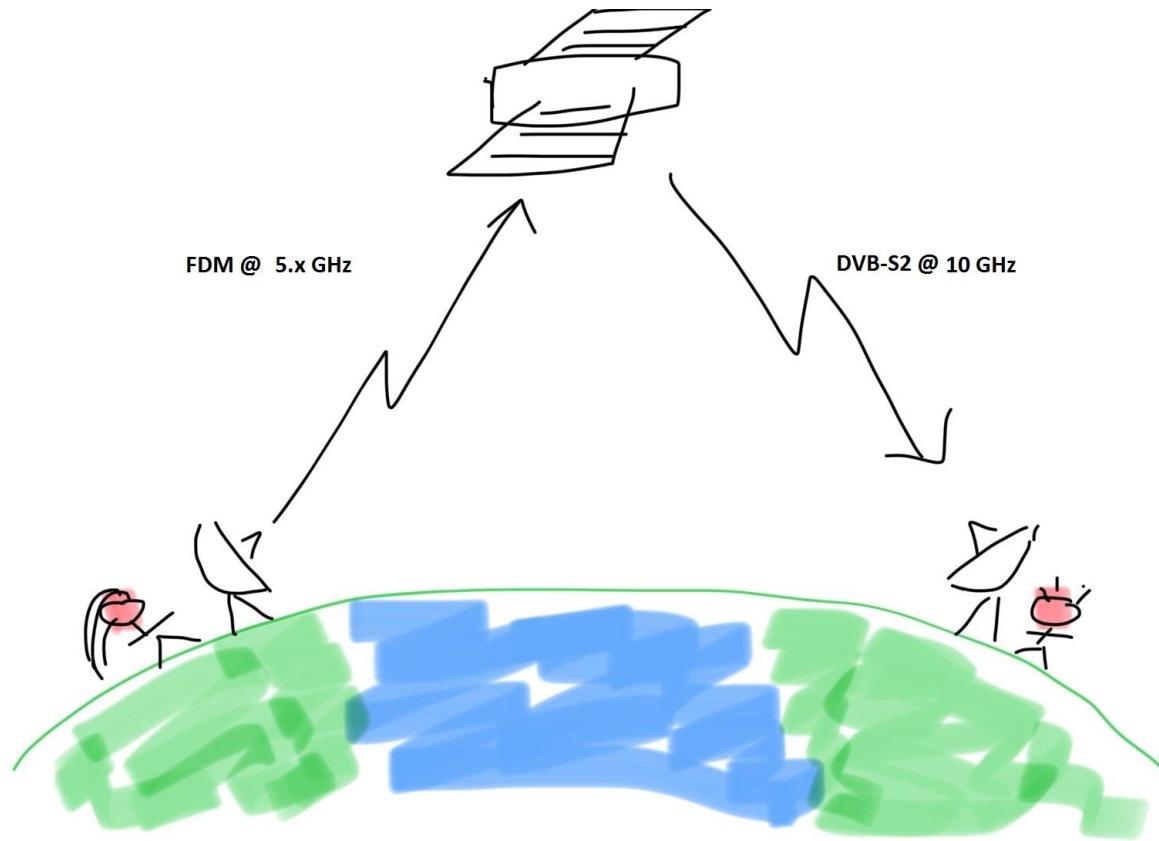
Into The Future

- By
- Charles Brain G4GUO
- CAT18 Sept 2018

Topics to be covered

- Phase 4 Ground and why we should be interested.
- Why Linear Amplifiers are not Linear
- Digital Pre-Distortion (DPD) basics
- My experiments with an MRF300AN on 71 MHz

Phase 4B Overview



DVB-S2/X usage differences

- Generic Stream Encapsulation (GSE). This allows IP traffic to be sent over the satellite.
- Adaptive Coding and Modulation (ACM). This allows different FEC and constellation combinations to be used on individual frames. The better groundstation you have the more bandwidth you will get.
- Uplink MSK

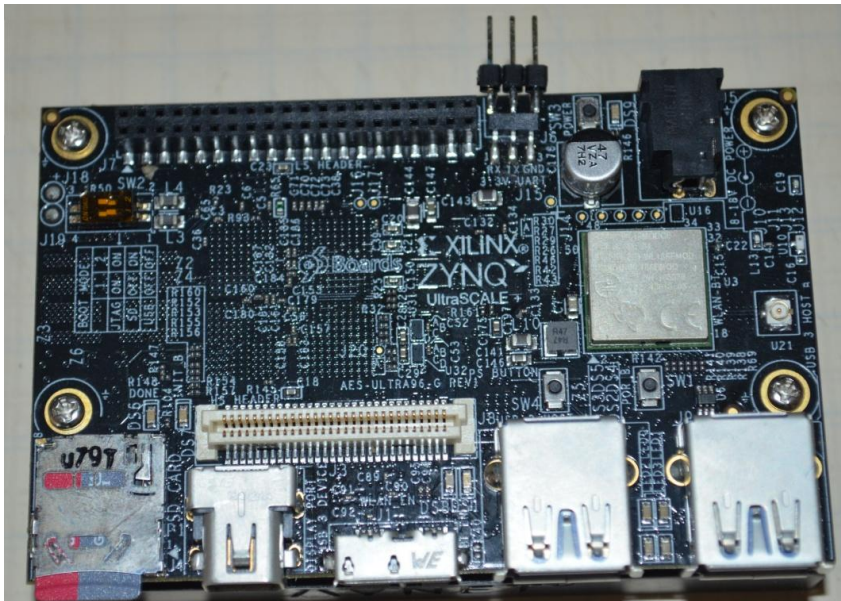
Ramifications

This will mean that an open source software modem needs to be developed that can run on multiple platforms, everything from a P.C down to a tiny embedded system. This is something we can use in the DATV community.

Current DVB-S2/X status

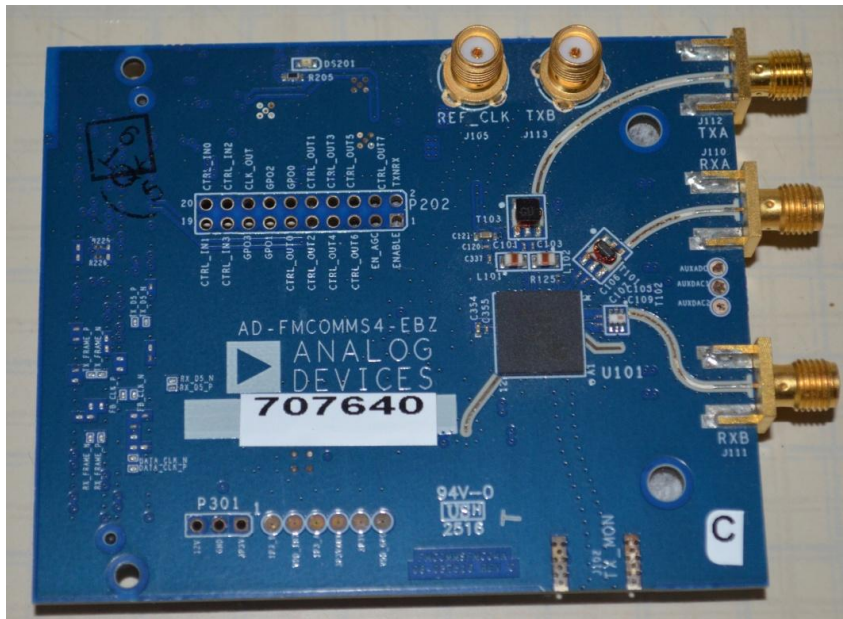
- I have been working on a GPU based Low Density Parity Check (LDPC) decoder using NVIDIA's CUDA environment.
- Later this week at GRcon18 there is a block party to develop DVB-S2 decoding modules for GNURadio. This will include an LDPC decoder.
- A low cost development system is being worked on using an ultra96 processor board and a FMCOMMS4 AD9364 evaluation board.

Ultra96 Embedded hardware



- XCZU3EG device
- Quad core A53 1.5 Ghz
- Dual core R5 600 Mhz
- Mali 400 667 Mhz
- 2G LPDDR4 memory
- 154K FPGA Logic cells
- 360 FPGA DSP Slices
- USB 2 and 3
- Display port
- WiFi
- Expansion headers
- SDSoC licence included
- \$249

FMCOMMS4



- AD9364
- FPGA Mezzanine Card (FMC)
- 1 Tx and 1 Rx channel
- 2.5 dB noise figure at 1 GHz
- 70 MHz to 6 GHz
- 56 MHz BW
- Only just enough IO pins on the ultra96

5.x GHz PA

- Currently investigating linear 400 mW driver stage base on Skyworks SE5004 device.
- Will move on to higher power stages later.

Final goal

- Single board transceiver 70 MHz – 6 GHz
- 10 GHz via LNB
- DVB-S2X software modem
- Networked interface
- Web based GUI

Digital Pre-Distortion (DPD)

- Or Why are Linear amplifiers not linear and what can be done about it?

Reasons for non-linearity

- Gain compression of the device (saturation etc) AM-AM characteristic
- Change in input and output capacitance due to bias voltage changes AM-PM characteristic
- DC bias shift due to self biasing, contributions from even order harmonic terms
- Harmonic distortion from baseband components
- Intermodulation distortion, mixing between fundamental and harmonics producing new output frequencies
- Cross-modulation between fundamental and harmonics producing new inband components
- Memory effects both short term and long term also will play a part
- Short term due to matching networks and device capacitance
- Long term due to thermal effects, charge trapping, bias circuit and control circuitry

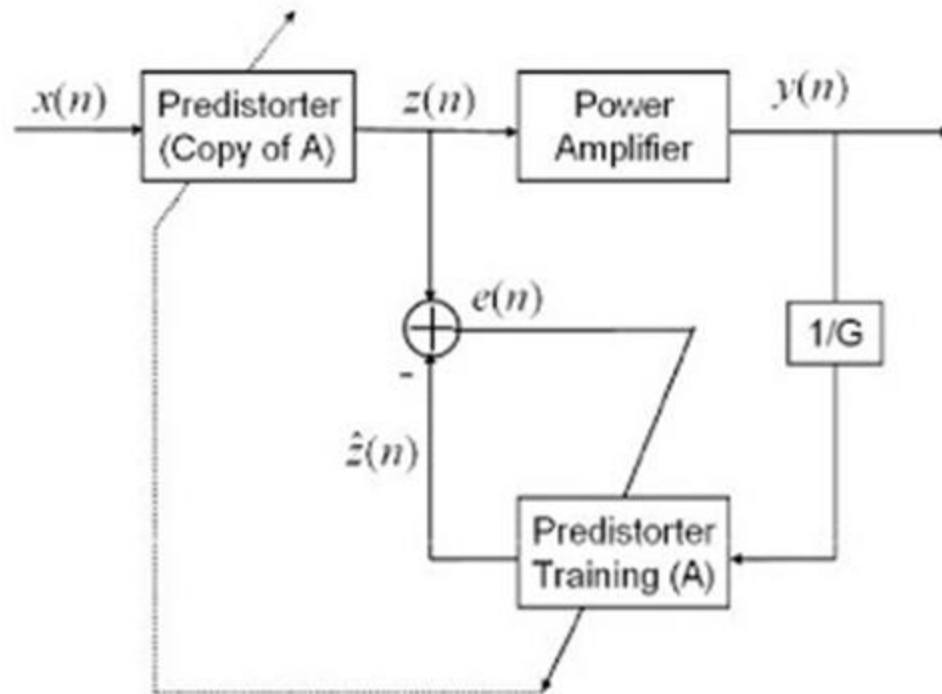
Hardware fixes

- Wideband decoupling of bias supplies to prevent even order products effecting the bias point
- Proper termination of the amplifiers harmonics

Software fixes

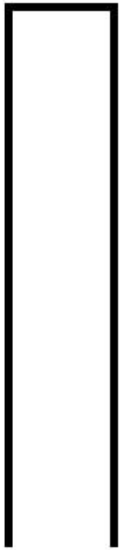
- Digital Pre-Distortion (DPD)
- A PA is a non linear system and therefore hard to model using linear maths.
- Need to convert this non linear problem into a linear problem so normal maths can be used
- Enter the Italian mathematician Vito Volterra (1860 – 1940) who worked on a branch of mathematics called functional analysis. He worked on the solution of intergral equations which later came to be known as “integral equations of the Volterra type”.
- Norbert Wiener picked up on Volterra’s techniques and applied them to analyse noise in radar systems. They were picked up again in the 1960s to model “weak” non linear systems.
- In a Linear amplifier “strong” non linearity starts to occur around the 1 dB compression point.
- The so called “Volterra series” is too computationally intensive to use directly so a simplified version which disposes of some terms in the series is now commonly used and is refered to as the “Memory Polynomial Model”
- This model is used to model the “weak” non linearity of an amplifier, then using a Least Mean Squares (LMS) approach a set of coefficients can be found that minimises that error using linear algebra.

Indirect Learning DPD

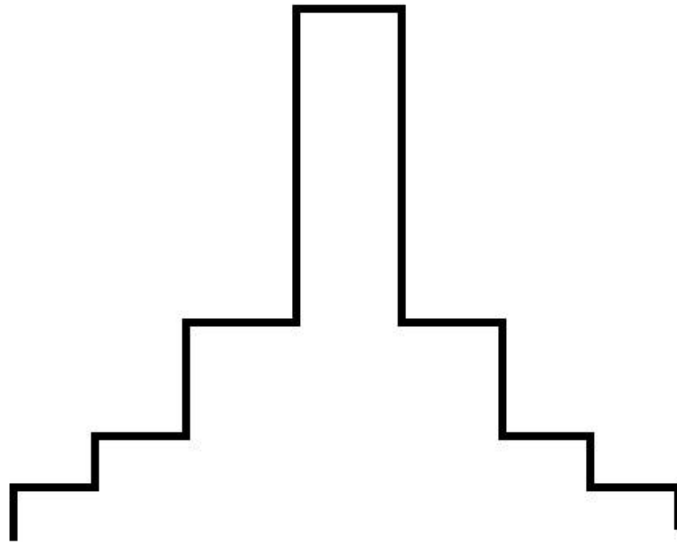


$$z(n) = \sum_{k=1}^K \sum_{q=0}^Q a_{kq} y(n-q) |y(n-q)|^{k-1}$$

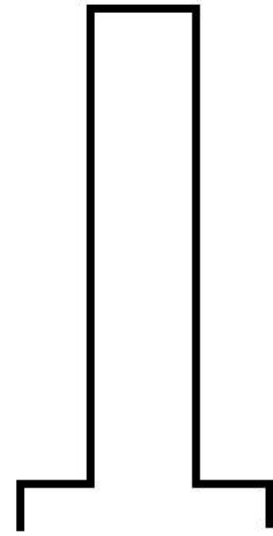
An act of faith?



Original



After Pre-Distortion



PA output

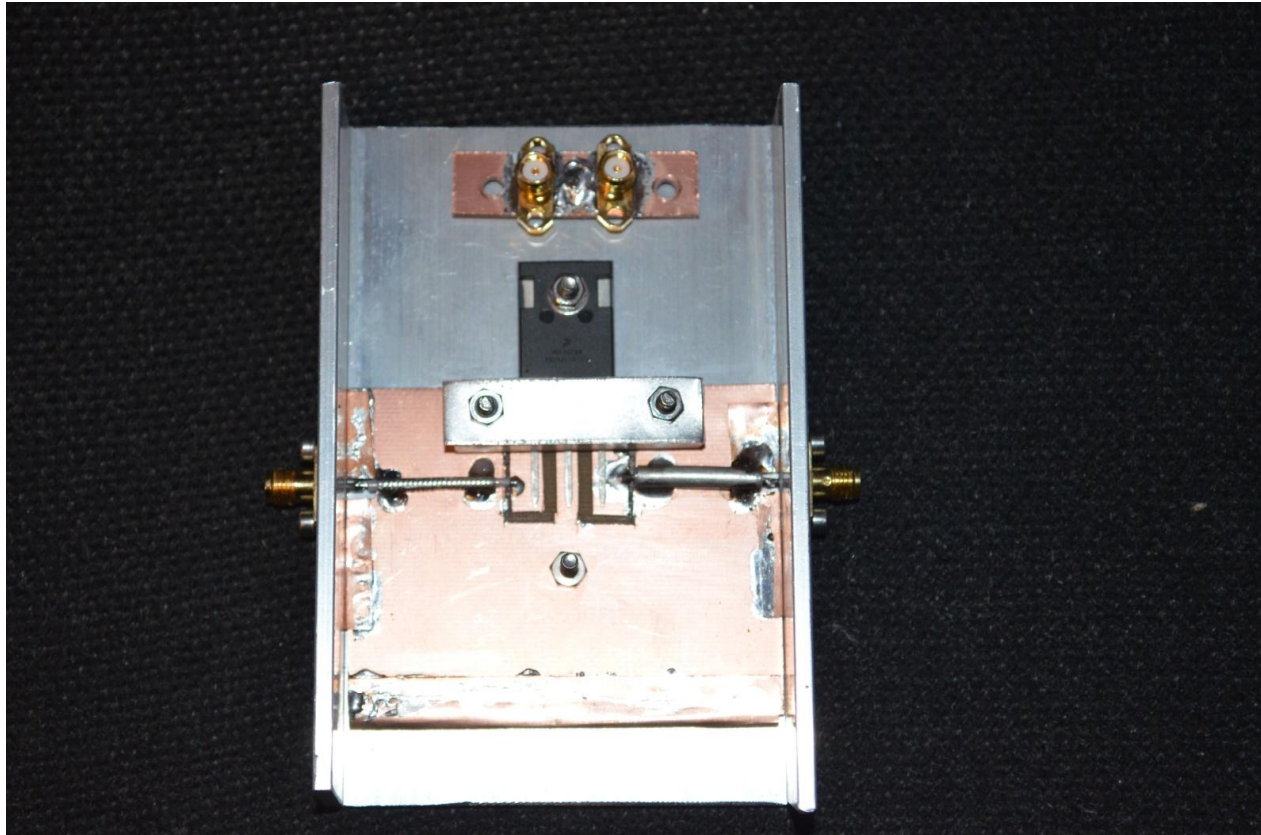
Practical DPD

- Both the transmitted signal and the monitored signal have to be oversampled (by a factor of 8 in my code) this so that the 3rd, 5th and 7th order IMD products can be captured. This means that currently only USB3 devices like the LimeSDR can be used as USB2 devices don't have the bandwidth that is required.
- Can only correct for “weak” non linearities so won't work if you drive your amplifier much past the 1 dB point.
- Should see between 10 – 20 dB improvement in the shoulders
- Maxim do a commercial RFPAL devboard SC2200-EVK2400 for around £400, it covers 2.3 – 2.7 GHz but has a minimum bandwidth of 1.2 MHz. It does the pre-distortion in the analogue domain but samples in the digital domain.

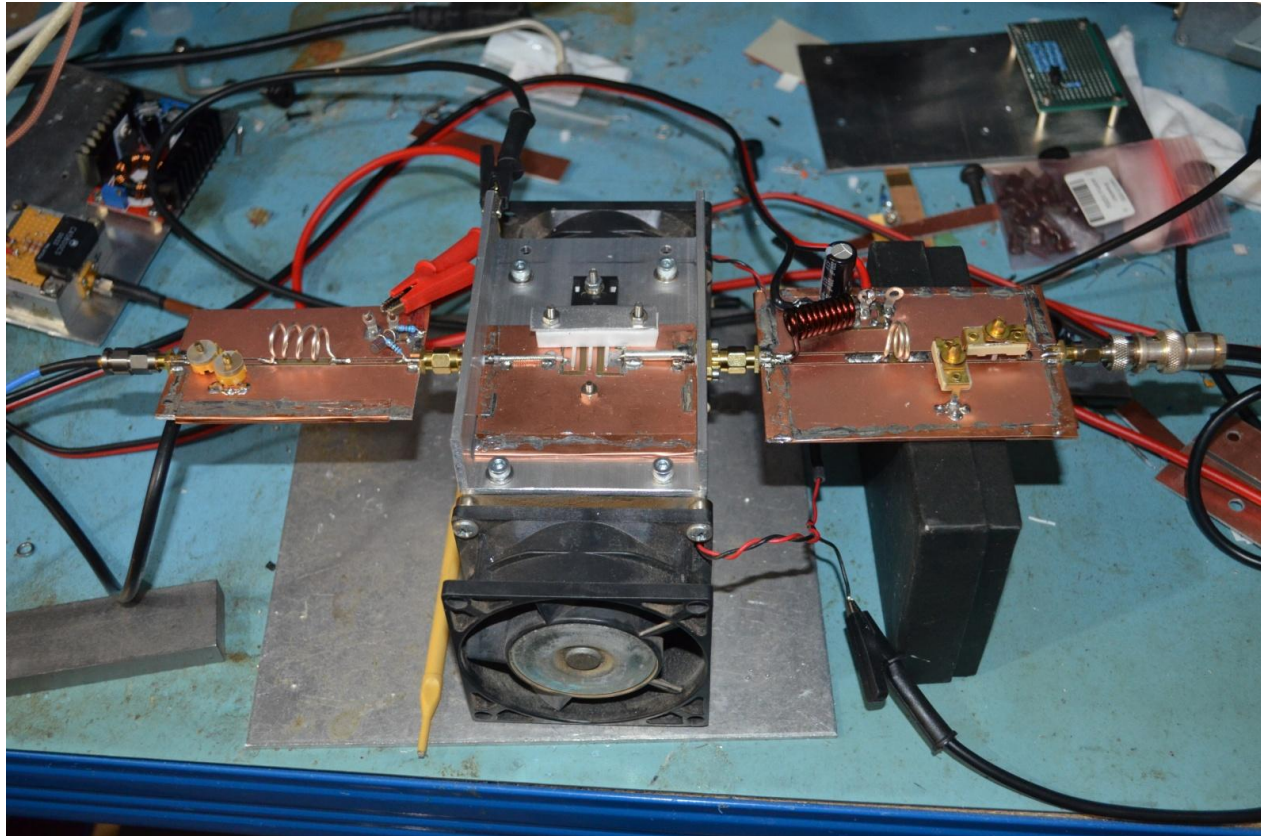
71.5 MHz Linear

- I thought I would have a go at designing an amplifier using the new NXP MRF300AN plastic transistors.
- These are 300 watt 250 MHz devices that require a 50v supply for best operation and can cope with a 60:1 VSWR
- I built a test jig that would allow me to match the device, then using a VNA measure the optimum match as seen by the device
- I was able to get 250 watts out of the device with an efficiency of 65% and about 40 watts of clean power, more than that required for the band.

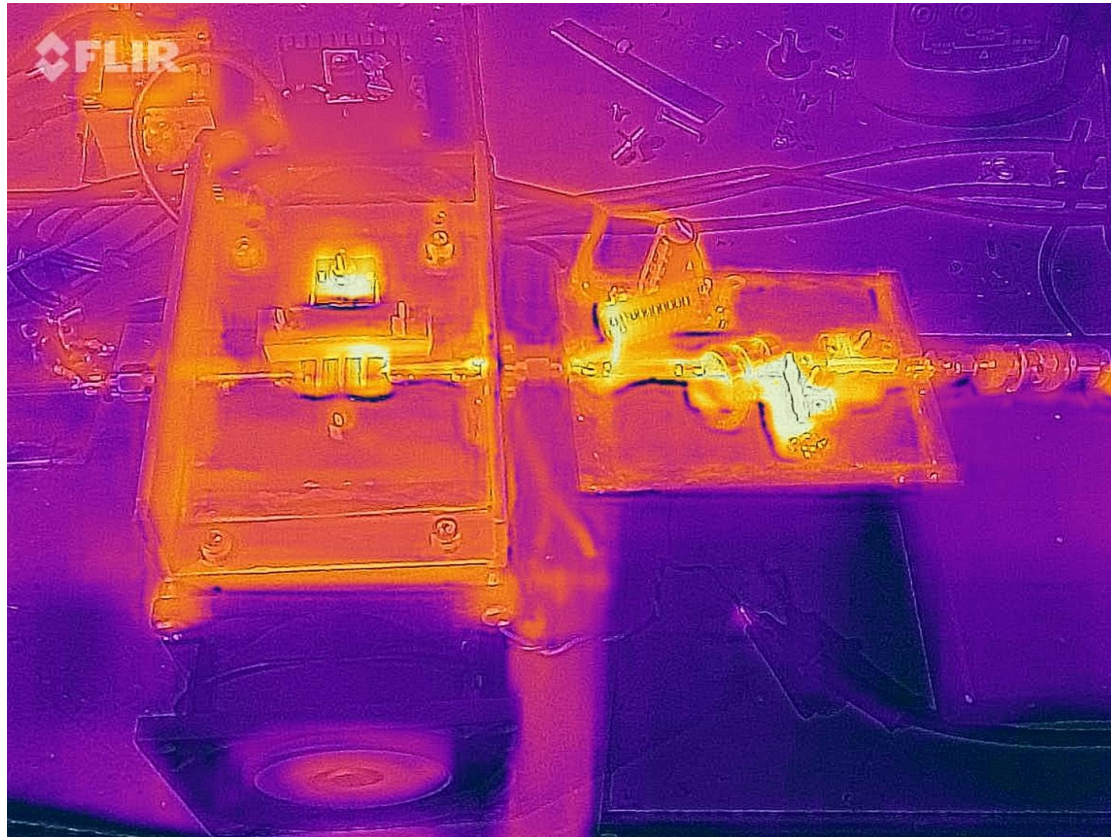
Test Jig



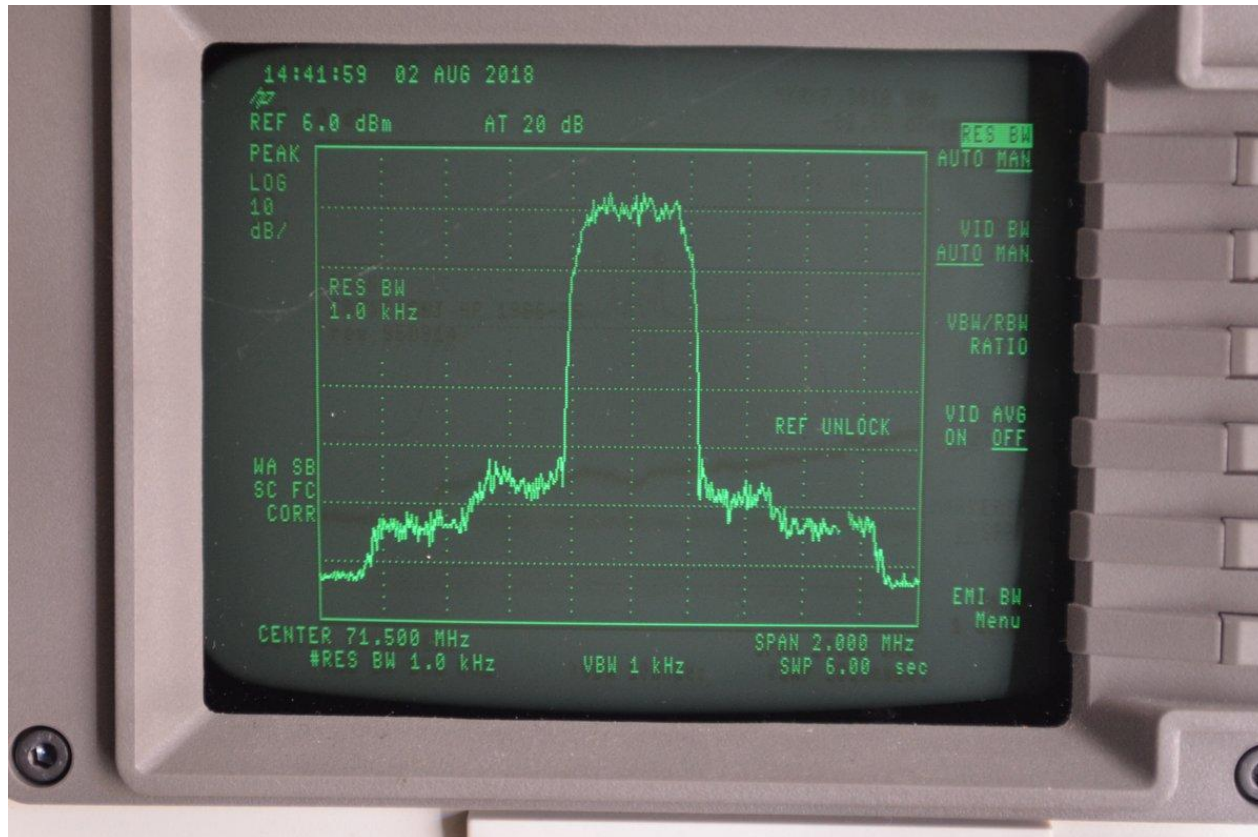
Device under test



Thermal Image



Output without DPD 40 watt level



Final Thoughts

- Initial idea was to develop an amplifier based on low cost parts that I could use to test DPD on.
- MRF300AN is too powerful for investigating DPD.
- Will probably use something like the G4BAO 1.3 GHz amplifier which is much easier to play with as power is quite low and being a higher frequency everything is more compact.
- The final solution would be to combine everything into a single board device based on the Xilinx range of MPSoC devices, some of which have hardware video codecs in them.

The End

- Thanks for watching
- Charles G4GUO